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TO: Mail Stop APPEAL BRIEF - PATENTS –
Commissioner for Patents – U.S. Patent Office

FAX NO.: (571) 273-8300

FROM: Robert M. Brush

DATE: October 23, 2006

MATTER: Serial No. 09/918,600 Filed: July 30, 2001

DOCKET NO.: C5048AP07

IN RE APPLICANT OF: Tseng et al.

The following has been received in the U.S. Patent and Trademark Office on the date of this facsimile:

X Reply Brief
Disclosure Statement & PTO-1449
Priority Document
X Response to Office Action Mailed August 24, 2006.
X Transmittal Letter
Fee Transmittal (2 copies)
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(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	18

Application Number	09/918,600
Filing Date	July 30, 2001
First Named Inventor	Tseng et al.
Art Unit	2128
Examiner Name	Akash Saxena
Attorney Docket Number	C5048AP07 (16503-302501)

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☑ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
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Remarks

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Moser IP Law Group		
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket No.: **C5048AP07**	§	Serial No.: **09/918,600**
Filed: **July 30, 2001**	§	Group Art Unit: **2128**
In re Application of: **Tseng et al.**	§	Confirmation No.: **8219**
	§	Examiner: **Saxena, Akash**

For: **Behavior Processor System and Method**

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

REPLY BRIEF

In response to the Examiner's Answer dated August 24, 2006, please enter this Reply Brief. As this response is submitted within two months from the date of mailing of the Examiner's Answer, Appellants believe that no fees are due in connection with this response. However, the Commissioner is hereby authorized to charge counsel's Deposit Account No. 50-3562 for any fees, including extension of time fees, required to make this response timely and acceptable to the Office.

STATUS OF CLAIMS

Claims 1-37 are pending in the application. Claims 1-37 were finally rejected in the Final Office Action mailed December 9, 2005. The rejection of claims 1-37 and the objection to claims 29 and 34 are presently appealed. The pending claims are shown in the attached Appendix.

STATUS OF AMENDMENTS

An amendment to claim 27 after final rejection has not been entered. Appellants note, however, that the amendment to claim 27 submitted after final was actually a duplicate of an amendment to claim 27 made in response to the first office action. Thus, it was not necessary to amend claim 27 after final rejection, since claim 27 had already been amended in identical fashion in response to the first office action.

SUMMARY OF CLAIMED SUBJECT MATTER

The Examiner stated that the summary of claimed subject matter in Appellants' appeal brief is deficient due to inconsistencies in definitions of claim terms and the relation of such claim terms to the specification and drawings. (Examiner's Answer, pp. 2-4). To clarify the claimed invention, Appellants set forth a supplemental summary of claimed subject matter, which also addresses the concerns of the Examiner in the Answer.

Aspects of the claimed invention may be understood with reference to pages 192-207 of the specification and FIGs. 99-105. In particular, hardware-based languages, such as VHDL, can be used to write code for simulation and code for synthesis. When writing code for simulation, various types of constructs can be used that cannot be used when writing synthesizable code. (Appellants' specification, p. 189, lines 13-24). These non-synthesizable constructs are referred to as "behavior functions." Examples of behavior functions include conditional operations (e.g., while...do loops, if...then...else loops, for loops, and the like), as well as behavioral instructions that conventionally processed in software because a hardware emulator has no place for them (e.g., $MONITOR, $DISPLAY, and $PRINT instructions). (Appellants' specification, p. 191, lines 9-25). Traditional accelerators and emulators do not address any behavior functions in hardware, but rather handle all such functions in software. Handling all behavior functions in software, however, exhibits drawbacks. (Appellants' specification, p. 191, lines 16-20 and lines 27-29; p. 192, lines 1-2).

Accordingly, in one embodiment of the invention, a behavior processor system is provided. A "behavior processor" is an FPGA device that can be programmed to provide any desired function(s) as known to those ordinarily skilled in the art. (Appellants' specification, p. 192, lines 4-5; p. 193, lines 17-19). Thus, the definition of "behavior processor" is clear. The behavior processor implements behavior functions in hardware, rather than software. (Appellants' specification, p. 189, lines 4-5; p. 192, lines 5-6; p. 192, line 28 through p. 193, line 5; p. 194, lines 18-28). Thus, contrary to the Examiner's assertion, it is clear that the behavior functions are implemented using hardware (i.e., an FPGA).

The behavior processor does work in conjunction with a software model. When the behavior processor determines that some condition provided by a behavior function is satisfied (e.g., if..then..else loop) that requires some intervention by a workstation or software model, the behavior processor sends a callback signal to the workstation or software model. (Appellants' specification, p. 189, lines 5-9; p. 192, lines 6-9; p. 204, lines 7-9). The callback signal is sent using a testbench callback process, which is described in the specification as a "call testbench primitive" or "axis_tbcall." "Once the condition is satisfied in hardware, the hardware emulator sends an interrupt-like signal back to the software processes for performing tasks associated with the testbench call." (Appellants' specification, p. 207, lines 5-7). Thus, contrary to the Examiner's assertion, some behavior functions are indeed implemented in hardware, as evidenced by the fact that the hardware determines if a condition provided by a behavior function is satisfied. (Appellants' specification, p. 206, line 26). The Examiner acknowledged that the condition is implemented in hardware (Examiner's Answer, p. 4). As noted above, the condition is an example of a behavior function. Thus, while some behavior functions may be performed by the software, some other behavior functions may be implemented in hardware by the behavior processor.

The Examiner did not agree with Appellants' mapping of the claim features to the figures. (Examiner's Answer, p. 4). Appellants clarify the mapping of claim features to the figures below.

Independent claim 1 recites (with reference numerals added)::

> A behavior processor system (FIG. 100) for operating a portion of a user design and interfacing with a host testbench process (3106), comprising:
>
> a reprogrammable logic element (3109) for modeling a hardware model of the portion of the user design that includes a behavior level function; and
>
> a testbench call back process (3109) for responding to the behavior level function in the reprogrammable logic element by sending a signal to the host testbench process.

The host test bench process is executed on the host workstation 3106. In an embodiment, the reprogrammable logic element is an FPGA, which is referred to as the behavior processor 3109a on a circuit board 3109. As described above, the behavior processor is configured to implement a behavior function (behavior level function) of a hardware model portion of the user design. The Examiner's assertion that the behavior level function is not in the reprogrammable logic element is incorrect, as detailed above. The behavior processor is also configured to implement a testbench call back process, as described above. The above-described mapping of claim 1 on the drawings is thus clear.

Finally, the Examiner stated that the language in claim 1 appears to lack a written description in the specification. It is not clear whether the Examiner is issuing a new rejection under 35 U.S.C. §112, or merely commenting that the summary is deficient. In any case, Appellants contend that claim 1 has support in the specification as detailed above and fully satisfies the written description requirement of §112.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Claims 29 and 34 are objected to for containing unclear language.

II. Claims 1-11, 13-15, 17-30, 32-34, and 36 stand rejected under 35 U.S.C. 102 (b) as anticipated by U.S. Patent No. 5,838,948 issued to Bunza.

III. Claims 4, 16, 31 and 35 stand rejected under 35 U.S.C. 103(a) as obvious over U.S. Patent No. 5,838,948 issued to Bunza in view of IEEE Std 1364-1995 "IEEE Standard Hardware Description Languange Based on the Verilog Hardware Description Language".

IV. Claims 12 and 37 stand rejected under 35 U.S.C. 103(a) as obvious over U.S. Patent No. 5,838,948 issued to Bunza in view of IEEE article "A 145MHz User-Programmable Gate Array" by Eduardo do Valle Simoes et al.

ARGUMENT

Response to Examiner's Answer

Appellants address the Examiner's "Response to Argument" below in the order such response appears in the Examiner's answer beginning on page 15 thereof.

I. Rejection of claims 29 and 34

The Examiner stated that claims 29 and 34 are "objected to under 35 U.S.C. §112, ¶2nd" and that such an objection cannot be appealed. (Examiner's Answer, p. 15). The refusal to grant claims because the subject-matter as claimed is considered unpatentable is known as a "rejection." MPEP 706.01. Rejections involve the merits of the claim and are thus subject to review by the Board. Id. A §112 rejection relates to the patentability of a claim and is thus can be appealed. To the extent that the Examiner is rejecting claims 29 and 34 under 35 U.S.C. §112, second paragraph, Appellants maintain the argument set forth in the appeal brief and respectfully request reconsideration by the Board.

II. Rejection of claims 1-11, 13-15, 17-30, 32-34, and 36 under §102(b)

The Examiner grouped the issues into Issues A through H. Issues A through D and H are addressed below. Appellants stand by the appeal brief with respect to Issues E, F, and G.

Issue A

The Examiner cited col. 5, lines 62-67 of BU'948, which states in part that hardware simulators allow multiple levels of abstraction from a switch or transistor level to a high level behavioral model. The cited portion, however, must be taken in context. The term "hardware simulator" as used in BU'948 refers to a software program that operates using a description of the target hardware. (BU'948, col. 5, lines 45-53). In fact, the cited portion is from the description of FIG. 1 in BU'948, which shows a conventional software-only simulator. (BU'948, col. 7, lines 8-9) (stating that "[t]he systems of FIGS. 1 and 2 simulate the target hardware completely in software."). Thus, the hardware simulator in BU'948 referenced by the Examiner does not teach or

suggest anything about a reprogrammable logic element that models a hardware portion of a user design.

The Examiner also cited col. 6, lines 10-13 of BU'948, which states in part that a processor functional model can be specified to various levels of abstraction by a conventional HDL. Again, the "processor functional model" as used in this section of BU'948 refers to a software model in the hardware simulator of FIG. 1. (BU'948, col. 6, lines 1-13). This cited portion is not relevant to a reprogrammable logic element that models a hardware portion of a user design.

The Examiner also cited col. 9, lines 8-12 of BU'948, which states in part that a hardware circuit emulator uses reconfigurable circuitry to emulate target circuitry functions in including ASIC or custom IC functions. Again, the cited portion must be taken in context. BU'948 goes on to state that use of such a hardware circuit emulator implies that the target hardware emulated by the reconfigurable circuitry has progressed very far along in the design process and thus precluding the use of unsynthesizable behavioral representations (i.e., behavior level functions or behavior functions as referred to in Appellants' specification). (BU'948, col. 5, lines 43-52). Thus, BU'948 explicitly states that this reconfigurable circuitry referenced by the Examiner cannot and does not model a hardware portion of a user design that includes a behavior level function, as recited in Appellants' claim 1.

From the above cited portions of BU'948; the Examiner concludes that BU'948 teaches that various abstraction levels including a behavioral level model can be put on a programmable logic element. However, the first two cited portions have noting to do with reprogrammable logic elements (hardware devices) and are thus not relevant. Only the last cited portion refers to reconfigurable circuitry, but BU'948 explicitly states that such circuitry does not model a user design that includes a behavior level function. Thus, the Examiner's assertion is clearly erroneous.

Finally, "behavioral synthesis," as known in the art, is a software process of synthesizing a behavioral description of a design (e.g., an HDL description) into a logical description (e.g., a gate-level description or netlist). That is, behavior synthesis converts one software representation of a circuit design into another software representation. Behavioral synthesis does not teach or suggest anything about a

hardware simulator or modeling a behavior function using a hardware device, such as an FPGA.

Issue B

The Examiner contends that since all patents are presumed valid and thus presumed enabled, BU'948 is valid and enabled. (Examiner's Answer, p. 17). Appellants have set forth an argument in the appeal brief to rebut the presumption that BU'948 is enabled for the particular disclosure at issue. The Examiner has not addressed the merits of Appellants' arguments, but rather has merely stated that BU'948 is presumed enabled. Appellants respectfully disagree as set forth in the appeal brief.

Issue C

The Examiner stated that Appellants' claim language does not provide a distinction between "synthesizable" and "non-synthesizable" behavioral functions and that arguments referring to these terms are moot. (Examiner's Answer, p. 18). First, the term "synthesizable behavioral function" is not used in BU'948. Appellants' reference to "unsynthesizable behavioral functions" is meant to relate the terms used by BU'948 to the term "behavior level function" used in Appellants' claims. BU'948 refers to "unsynthesizable behavioral representations," which are equivalent to Appellants' "behavior level functions". BU'948 states that such behavior representations are precluded by the use of hardware emulators. In contrast to this statement, the Examiner is arguing that BU'948 does teach a reprogrammable logic element for modeling a hardware portion of the user design having a behavior level function. Appellants refer to the "unsynthesizable behavior functions" of BU'948 to show that the Examiner's argument is erroneous.

The Examiner cited BU'948, col. 9, lines 49-52, which states that "use of unsynthesizable behavioral or high-level design representations, typical of early states of design, are precluded by the use of hardware emulators." (Examiner's Answer pp. 18). From this negative statement, the Examiner asserts that BU'948 positively teaches modeling behavioral functions in hardware in general. Nowhere in the cited portion

does BU'948 positively state that behavioral functions can be used with hardware emulators. Note that modeling behavioral functions in hardware in general is the inverse of what is actually taught in BU'948. Since the inverse of a proposition is not necessarily true, BU'948 cannot inherently teach modeling behavioral functions in hardware in general.

Finally, Appellants have set forth support for modeling behavior level functions in hardware above in the summary. The Examiner has not set forth any specific reason why the "statements" in Appellants' specification are non-enabling and thus has not set forth a prima facie case for lack of enablement. Namely, the Examiner has not set forth a rational basis as to why Appellants' specification does not teach the claimed invention to one of ordinary skill in the art without undue experimentation, nor has the Examiner set forth any basis for doubting the objective truth of the statements in the specification that purport to teach the claimed invention. As noted above, the condition is an example of a behavior function. Thus, while some behavior functions may be performed by the software, some other behavior functions may be implemented in hardware by the behavior processor.

Issue D

The Examiner next cites col. 13, line 55 through col. 14, line 23 of BU'948 for teaching use of a reprogrammable logic element to model a hardware portion of a user design having a behavior level function that is a condition. (Examiner's answer, p. 20). The cited portion is from the description of FIG. 6 in BU'948 and refers to the "processor emulator." BU'948 states that operation of the processor emulator is similar to that of the conventional hardware emulators illustrated in FIG. 4 except for "operation of the control circuit". As discussed above with respect to Issue A, the conventional hardware emulators described by BU'948 do not model a hardware portion of a user design that includes a behavior level function. Thus, unless the "operation of the control circuit" in BU'948 teaches modeling a hardware portion of a user design that includes a behavior level function, the processor emulator of FIG. 6 in BU'948 does not teach or suggest the reprogrammable logic element in Appellants' claims.

The "operation of the control circuit" in BU'948 does not teach or suggest modeling a hardware portion of a user design that includes a behavior level function. In FIG. 6 of BU'948, a microprocessor portion of the hardware design (referred to as the target microprocessor) is modeled by the processor emulator, and additional processor-related circuitry (referred to as target circuitry) is modeled by a hardware simulator (software simulator). (BU'948, col. 10, lines 20-35). The control circuit referred to by the Examiner "provides hardware capability to detect events requiring the interaction of the target microprocessor and the target circuitry." (BU'948, col. 13, line 66 through col. 14, line 2). While the control circuit identifies "conditions," these conditions have nothing to do with a condition that is a behavior level function in a user design.

Issue H

The Examiner stated that there is no clear definition of "behavior processor" in Appellants' specification. (Examiner's answer, p. 25). As clarified above in the supplemental summary, a "behavior processor" is an FPGA device that can be programmed to provide any desired function(s) as known to those ordinarily skilled in the art. The behavior processor implements behavior functions in hardware, rather than software. In light of this clarification, the behavior process of Appellants' invention is clearly different that the processor emulator of BU'948. As discussed above, the processor emulator of BU'948 does not model behavior functions in hardware.

III. Rejection of claims 4, 16, 31, and 35 under 35 U.S.C. §103(a)

The Examiner has used BU'948 as the primary reference in rejecting dependent claims 4, 16, 31, and 35. As discussed in the appeal brief and above, BU'948 is deficient in teaching or suggesting the invention recited in Appellants' independent claims. Since the Examiner is not relying on IEEE1364 to teach or suggest a reprogrammable logic element that models a hardware portion of a user design having a behavior level function, and since BU'948 is devoid of any such teaching or suggestion, no conceivable combination of BU'948 and IEEE1364 renders obvious Appellants' invention.

IV. Rejection of claims 12 and 37 under 35 U.S.C. §103(a)

The Examiner has used BU'948 as the primary reference in rejecting dependent claims 12 and 37. As discussed in the appeal brief and above, BU'948 is deficient in teaching or suggesting the invention recited in Appellants' independent claims. Since the Examiner is not relying on ED1995 to teach or suggest a reprogrammable logic element that models a hardware portion of a user design having a behavior level function, and since BU'948 is devoid of any such teaching or suggestion, no conceivable combination of BU'948 and ED1995 renders obvious Appellants' invention.

CONCLUSION

For the reasons advanced above, Appellants respectfully urge that the rejections of claims 1-37 as being unpatentable are improper. Reversal of the rejections in this appeal is respectfully requested.

Respectfully submitted,

10-22-06

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CLAIMS APPENDIX

1. (Original) A behavior processor system for operating a portion of a user design and interfacing with a host testbench process, comprising:

a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavior level function; and

a testbench call back process for responding to the behavior level function in the reprogrammable logic element by sending a signal to the host testbench process.

2. (Original) The system of claim 1, wherein the behavior level function includes a condition.

3. (Previously Presented The system of claim 2, wherein the behavior level function includes a condition and the occurrence of the condition triggers the testbench call back process.

4. (Original) The system of claim 2, wherein the condition includes an "if-then" conditional statement implemented in hardware.

5. (Original) The system of claim 1, wherein the signal includes an interrupt from the testbench call back process to the host testbench process.

6. (Original) The system of claim 1, wherein the signal includes an interrupt from the reprogrammable logic element to the host testbench process.

7. (Original) The system of claim 1, wherein the signal includes data from the testbench call back process to the host testbench process.

8. (Previously Presented) The system of claim 1, wherein a reprogrammable logic element temporarily suspends operation upon the occurrence of the condition.

9. (Original) The system of claim 8, wherein the reprogrammable logic element resumes operation from the point at which operation was temporarily suspended upon the service of the signal by the host testbench process.

10. (Original) The system of claim 2, wherein the reprogrammable logic element temporarily pauses operation upon the occurrence of the condition.

11. (Original) The system of claim 1, wherein the reprogrammable logic element includes a clock that controls the speed of processing instructions and data in the reprogrammable logic element.

12. (Original) The system of claim 11, wherein the clock runs at 20 MHz.

13. (Original) A verification system for analyzing a user design, comprising:

a host workstation for modeling and operating a software model of the user design;

a reprogrammable hardware emulator for modeling a first hardware model of at least a portion of the user design; and

a behavior processor for modeling a second hardware model of a selected portion of the user design.

14. (Original) The verification system of claim 13, wherein the selected portion includes a behavioral aspect of the user design.

15. (Original) The verification system of claim 13, wherein the selected portion includes at least one condition in the user design.

16. (Original) The verification system of claim 15, wherein the at least one condition includes an "if- then" conditional statement.

17. (Original) The verification system of claim 13, wherein the behavior processor includes a testbench callback process for responding to the selected portion of the user design modeled in the reprogrammable hardware emulator by sending a signal to the host workstation.

18. (Previously Presented) The verification system of claim 13, wherein the selected portion includes at least one condition in the user design and the behavior processor includes a testbench callback process for responding to the at least one occurrence of the condition in the reprogrammable hardware emulator by sending a signal to the host workstation.

19. (Original) The verification system of claim 18, wherein the reprogrammable hardware emulator temporarily suspends operation upon the occurrence of the condition.

20. (Original) The verification system of claim 19, wherein the reprogrammable hardware emulator resumes operation from the point at which operation was temporarily suspended upon the service of the signal by the host workstation.

21. (Original) The verification system of claim 18, wherein the reprogrammable hardware emulator temporarily pauses operation upon the occurrence of the condition.

22. (Previously Presented) The verification system of claim 13, wherein the selected portion includes at least one condition for the user design and the behavior processor sends a wait signal to the reprogrammable hardware emulator upon the at least one occurrence of the condition so that the reprogrammable hardware emulator temporarily suspends operation.

23. (Original) The verification system of claim 22, wherein the behavior processor sends a resume signal to the reprogrammable hardware emulator upon the service of

the signal by the host workstation so that the reprogrammable hardware emulator resumes operation from the point at which operation was temporarily suspended.

24. (Original) The verification system of claim 22, wherein the behavior processor toggles the wait signal to the reprogrammable hardware emulator upon the service of the signal by the host workstation so that the reprogrammable hardware emulator resumes operation from the point at which operation was temporarily suspended.

25. (Original) The verification system of claim 13, wherein the behavior processor operates when it receives a request for service from the host workstation.

26. (Original) The verification system of claim 13, wherein the behavior processor operates when it receives a request for service from the reprogrammable hardware emulator.

27. (Previously Presented) A method of verifying a user design where the verification environment includes a host workstation for running a simulation of the user design and a testbench process, comprising steps:

modeling a behavioral portion of the user design in hardware, where the behavioral portion includes a service request; and

sending a signal to the testbench process in the host workstation upon the occurrence of the service request.

28. (Original) The method of claim 27, further comprising step:
suspending the operation of the simulation until the host workstation services the signal.

29. (Original) The method of claim 27, further comprising step:
suspending the operation of the simulation until the testbench process services the signal.

30. (Original) The method of claim 27, wherein the step of modeling the behavioral portion includes modeling conditional statements.

31. (Previously Presented) The method of claim 30, wherein the step of modeling the conditional statements includes "if-then" statements.

32. (Original) A method of verifying a user design where the verification environment includes a host workstation for running a simulation of the user design and a testbench process, comprising steps:

modeling a conditional portion of the user design in a hardware environment;

executing the conditional portion in the hardware environment; and

sending an interrupt to the testbench process in the host upon the occurrence of at least one condition in the conditional portion.

33. (Original) The method of claim 32, further comprising step:
suspending the operation of the simulation until the host workstation services the interrupt.

34. (Original) The method of claim 32, further comprising step:
suspending the operation of the simulation until the testbench process services the interrupt.

35. (Previously Presented) The method of claim 32, wherein the step of modeling the conditional portion includes "if-then" statements.

36. (Original) The method of claim 32, wherein the step of executing occurs at the speed of a hardware clock.

37. (Original) The method of claim 36, wherein the step of executing occurs at 20 MHz.